# IN THE CLAIMS

Please amend the claims as follows.

For the Examiner's convenience, a list of all claims is included below.

1.     (Original)  A method comprising:

reading a time of exiting a reduced power consumption state prior to an

execution of an interrupt routine;

storing the time of exiting the reduced power consumption state in a

register; and

calculating a reduced power consumption state duration based on the time of

exiting the reduced power consumption state stored in the register.

2.     (Currently Amended)  The method of claim 1 wherein the reduced power

consumption state is a~~ C1 power state~~ <u>entirely responsive to the interrupt routine</u>.

3.     (Original)  The method of claim 1 furthering comprising:

reading a time of entering the reduced power consumption state;

storing the time of entering the reduced power consumption state in a main

memory; and

calculating the reduced power consumption state duration utilizing the time

of entering and the time of exiting the reduced power consumption state.

4.     (Cancelled)

5.      (Original)  The method of claim 1 wherein the register is located in a

processor.


6-47    (Cancelled)


48.     (Previously Presented)  An apparatus comprising:

an operating system to read a time of entering a reduced power consumption

state, and

to read a time of exiting the reduced power consumption state prior to an

execution of an interrupt routine; and

a main memory to store the time of entering.


49.     (Currently Amended)  The apparatus of claim [[20]] 48 further comprising a

chip to store the time of exiting the reduced power consumption state in a register.


50.     (Previously Presented)  The apparatus of claim 48 further comprising a

processor to store the time of exiting the reduced power consumption state in a

register.


51.     (Previously Presented)  The apparatus of claim 49 wherein the operating

system further operates to perform a cycle to the chip.

52.     (Previously Presented)  The apparatus of claim 48 wherein the operating

system further operates to calculate a reduced power consumption state duration.


53.     (Currently Amended)  The apparatus of claim 48 wherein the reduced power

consumption state is a C1 power state entirely responsive to the interrupt routine.


54.     (Currently Amended)  An apparatus comprising:

        an operating system to request a chip to store a time of entering a reduced

power consumption state and a time of exiting the reduced power consumption

state; and

        the chip to store the time of entering and the time of exiting the reduced

power consumption state in a register and to automatically calculate a reduced

power consumption state duration.


55.     (Currently Amended)  The apparatus of claim 54 wherein the reduced power

consumption state is a C1 power state entirely responsive to the interrupt routine.


56.     (Previously Presented)  An apparatus comprising:

        means for reading a time of exiting a reduced power consumption prior to

an execution of an interrupt routine;

        means for storing the time of exiting the reduced power consumption state

in a register; and

        means for calculating a reduced power consumption state duration.

57. (Previously Presented) The apparatus of claim 56 further comprising:

means for reading a time of entering the reduced power consumption state;

means for storing the time of entering the reduced power consumption state

in a main memory; and

means for calculating the reduced power consumption state duration

utilizing the time of entering and the time of exiting.

58. (Currently Amended) The apparatus of claim 56 wherein the reduced power

consumption state is ~~C1 power state~~ <u>entirely responsive to the interrupt routine.</u>

59. (Previously Presented) The apparatus of claim 56 wherein the register is

located in a personal computer chipset.

60. (Previously Presented) The apparatus of claim 56 wherein the register is

located in a processor.